Homework 4

(Due date: November 20th @ 5:30 pm)
Presentation and clarity are very important! Show your procedure!

PROBLEM 1 (20 PTS)

- Using the HCS12D PWM Module, write a C program (*provide a printout*) to generate a 24 KHz signal with a 30% duty cycle on PP5. E-clock = 24 MHz. Indicate the period of the clock source of PWM5.

PROBLEM 2 (20 PTS)

- HCS12D – SCI1: Complete the following table. E-clock = 24 MHz.

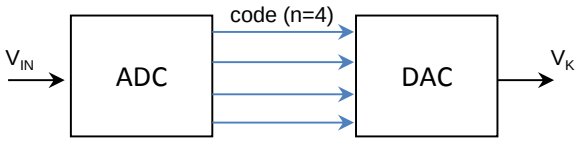
Baud Rate = Tx clock frequency (Hz)	**Rx clock frequency** (Hz)	**SCI1BDH**	**SCI1BDL**
375000			
	24000		
20000			
		1D	4C
	8000		

  - ✓ What are the largest and smallest Baud Rates? Provide the respective values of `SCI1BDH` and `SCI1BDL` on each case.

- HCS12D – SPI0 with the LTC1661 DAC: Using the function `sendLTC1661(char x1, char x2)` found in `unit10a.c`, what are the two pairs of 8-bit values (x1, x2) that should be written in order to have 2.8v on Output B of the DAC (use the datasheet)? Also, if a Baud Rate of $4x10^6$ is desired (E-clock=24 MHz), what is the value of `SPI0BR`?

PROBLEM 3 (20 PTS)

- Analog to Digital Conversion. Using the successive approximation algorithm with n=4 (codes from `0000` to `1111`), compute the 4-bit codes and the quantized voltages V_k for the following input voltages. V_{DD} = 5v.
  Formula for Quantized voltage: $V_k = \left(\frac{k}{2^n}\right) V_{DD}$



Vin (v)	**4-bit code**	**V_k (v)**
4.78		
0.31		
2.67		

  - ✓ What is the maximum possible quantization error (in voltage units) with n=4?

- HCS12D: For E-clock=24 MHz and n=10, what is the minimum conversion time? Indicate the value of `ADTnCTL4` that achieves this.

PROBLEM 4 (40 PTS)

- Attach a printout of your Project Status Report (no more than three pages, single-spaced, 2 columns). This report should contain the current status of the project. Use the provided template (`Final Project – Report Template.docx`).